

**CLAIMS**

Applicants respectfully request that the following claim amendments be entered:

1. (Cancelled).
2. (Currently Amended) The microprocessor of Claim 18, further comprising:  
a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;  
a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time.
3. (Currently Amended) The microprocessor of Claim 18, further comprising:  
a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;  
a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time; and  
a dynamic clock-control unit connected to at least the first local clock buffer for providing a first control signal to at least the first local clock buffer and configured for generating the first control signal, the first control signal enabling the first clock signal to be operational only during the first period of time.
4. (Currently Amended) The microprocessor of Claim 18, further comprising an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic.
5. (Currently Amended) The microprocessor of Claim 18, further comprising:

an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic;

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time; and

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time.

6. (Currently Amended) The microprocessor of Claim 18, wherein the first stage comprises one or more latches, and wherein the second stage comprises one or more latches.

7. (Currently Amended) The microprocessor of Claim 18, further comprising an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic, wherein the integrated storage component comprises an array.

8. (Currently Amended) The microprocessor of Claim 18, wherein the second period of time is automatically determined by delaying the first period of time by one cycle of the main processor clock.

9. (Currently Amended) The microprocessor of Claim 18, further comprising:  
an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic;

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time; and

a dynamic clock-control unit connected to at least the first local clock buffer for providing a first control signal to at least the first local clock buffer and configured for generating the first control signal, the first control signal enabling the first clock signal to be operational only during the first period of time.

10. (Currently Amended) The microprocessor of Claim 18, wherein each storage component in the first stage comprises:

a master latch configured for storing the operand data and being clocked by a first master clock derived from the first clock; and

a slave latch connected to the master latch for receiving the operand data from the master latch and storing the operand data, the slave latch being configured for being clocked by a first slave clock derived from the first clock.

11-17. (Cancelled).

18. (Previously Presented) A microprocessor configured for executing at least one instruction, the microprocessor having a main processor clock, the microprocessor comprising:

a first stage having one or more storage components configured for storing operand data of the at least one instruction, the first stage being clocked by at least a first clock derived from the main processor clock;

a first combinatorial logic connected to the first stage for receiving the operand data from the first stage and configured for processing the operand data and generating first output data, wherein the first clock is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

a second stage of one or more storage components configured for storing the first output data, the second stage being clocked by at least a second clock derived from the main processor clock;

control logic that is at least configured to:

generate at least two instruction-valid control bits, wherein the at least two instruction-valid control bits are configured to:

disable the first clock derived from the main processor clock by a first instruction-valid control bit if a first stage is unused or disable the second clock derived from the main processor clock by a second instruction-valid control bit if a second stage is unused;

enable the first clock and the second clock in response to a scan mode signal;

disable the first clock by the first instruction-valid control bit in response to a first stop control signal and disable the second clock by the second instruction-valid control bit in response to a second stop control signal; and

a second combinatorial logic connected to the second stage for receiving the first output data from the second stage and configured for processing the first output data and generating second output data, wherein the second clock is operational only during a second period of time when the first output data is processed by the second combinatorial logic.